CLAIMS

1. A method for regulating a decision threshold in a sampling of a binary signal by evaluation of error correction signals, the method comprising the steps of:

counting both a number of 1-bits detected as erroneous and a number of 0-bits detected as erroneous;

evaluating the number of 1-bits detected as erroneous and the number of 0-bits detected as erroneous; and

adjusting the decision threshold correspondingly to achieve an optimum ratio of the number of 1-bits detected as erroneous and the number of 0-bits detected as erroneous.

2. A method for regulating a decision threshold in a sampling of a binary signal as claimed in claim 1, the method further comprising the steps of:

forming a difference between the number of 1-bits detected as erroneous and the number of 0-bits detected as erroneous; and

converting the difference into an actuating signal for the decision threshold.

3. A method for regulating a decision threshold in a sampling of a binary signal as claimed in claim 2, the method further comprising the step of setting the decision threshold, for balanced codes, such that the difference becomes zero.

4. A method for regulating a decision threshold in a sampling of a binary signal as claimed in claim 2, the method further comprising the step of taking into account, for unbalanced codes, a ratio of a total number of 1-bits to a total number of 0-bits of the binary signal.

5. A method for regulating a decision threshold in a sampling of a binary signal as claimed in claim 4, the method further comprising the steps of:

forming a first ratio of the number of 1-bits detected as erroneous to the total number of 0-bits;

forming a second ratio of the number of 0-bits detected as erroneous to the total number of 1-bits;

comparing the first and second ratios; and

setting the decision threshold based on the comparison such that a difference between the first and second ratios becomes zero.

6. A method for regulating a relative phase of a sampling clock signal with respect to a phase of a binary signal by evaluation of error correction signals, the method comprising the steps of:

counting and evaluating a number of bits detected as erroneous before a transition between binary states and a number of bits detected as erroneous after a transition between the binary states; and

adjusting the phase of the sampling clock signal such that at least approximately the same number of bits detected as erroneous occurs before and after the transition between the binary states.

7. A method for regulating a relative phase of a sampling clock signal with respect to a phase of a binary signal as claimed in claim 6, wherein evaluation only occurs for at least one of transitions for specific binary sequences and a specific transition between the binary states.

8. A method for regulating a relative phase of a sampling clock signal with respect to a phase of a binary signal as claimed in claim 6, wherein the error correction signals of an error correction device are at least one of evaluated in a manner logically combined with the respective binary state of a bit detected as erroneous and evaluated before and after the transition between the binary states as phase correction signals.

9. A method for regulating a relative phase of a sampling clock signal with respect to a phase of a binary signal as claimed in claim 6, wherein a decision threshold for the binary signal and the phase of the sampling clock signal are regulated.

10. A method for regulating a relative phase of a sampling clock signal with respect to a phase of a binary signal as claimed in claim 6, wherein a proportion of bits detected as erroneous is used for controlling a time constant of a regulating system.

11. A system for regulating a decision threshold of a data regenerator having a decision stage, to which a binary signal and a comparison signal are fed, the system comprising:

a sampling flip-flop having a data input connected to an output of the decision stage;

a controllable clock regenerator which generates a sampling clock signal for the sampling flip-flop;

an error correction device for controlling the controllable clock regenerator; and

a regulator, a first correction signal being fed to the regulator from the error correction device which indicates a correction of a 1-bit, and a second correction signal being fed to the regulator from the error correction device which indicates a correction of a 0-bit, wherein the regulator separately sums and assesses the first and second correction signals and generates a control signal which determines a magnitude of the comparison signal.

12. A system for regulating a decision threshold of a data regenerator as claimed in claim 11, wherein a phase of the sampling clock signal is also regulated.

13. A system for regulating a phase of a sampling clock signal, the system comprising:

a clock regenerator for generating the sampling clock signal;

an error correction device for controlling the clock regenerator;

a sampling flip-flop into which a binary signal is latched via the sampling clock signal; and

a regulator, a first phase correction signal being fed to the regulator from the error correction device which indicates a correction of a bit before a signal transition between two binary states, and a second phase correction signal being fed to the regulator which indicates a correction of a bit after a signal transition between two binary states, the regulator counting the correction signals and comparing the sums to generate a phase correction signal which generates the phase of the sampling clock signal such that at least approximately a same number of correction signals occurs before and after a transition between the binary state.

14. A system for regulating a phase of a sampling clock signal as claimed in claim 13, wherein a decision threshold of the sampling clock signal is also regulated.